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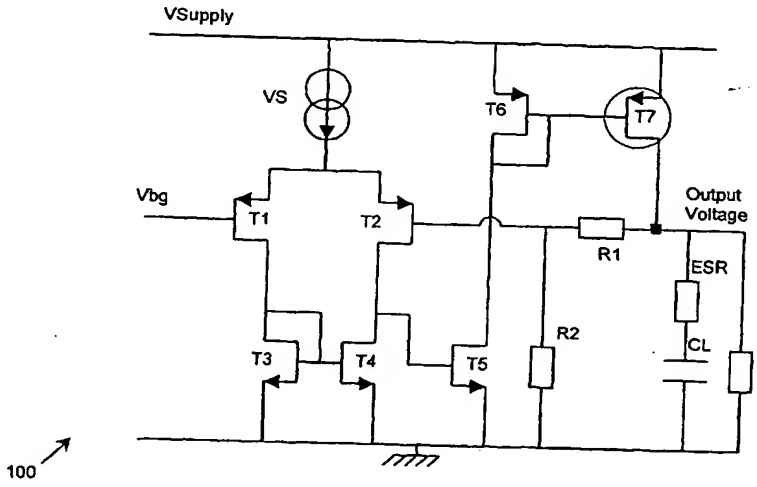
(54) Title: LOW DROP-OUT VOLTAGE REGULATOR AND METHOD



(57) Abstract: A low drop-out voltage regulator (300) and method comprising: a differential transistor arrangement (Q1-Q2) for receiving a reference voltage and in dependence thereon producing a regulatred output voltage; an output stage (Q3) for coupling to a load; and a control loop (310) coupled to the differential transistor arrangement for providing a dominant pole. Since a load capacitance is not used for dominant pole, stability of operation may be obtained with a lower load capacitance. The output stage is preferably a closed-loop unity gain amplifier providing a low impedance output. This provides the following advantages: 1 - The output capacitor can be dramatically reduced or removed (a low dominant pole, allows the regulator to worth with 0nF output capacitor). 2 - internal power consumption can be reduced, improving regulator efficiency. 3 - Low output impedance is provided, with very low DC output resistance. 4 - The load capacitor can have zero ESR (equivalent serial resistance).

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